

CLAIMS

WHAT IS CLAIMED IS:

1. An assembly, comprising:
 - 2 a printed circuit assembly with a pad layout pattern; and
 - an area array package with a pad layout pattern attached to the
 - 4 printed circuit assembly; wherein at least one of the pad layout of the printed
 - circuit assembly or the pad layout of the area array package has an offset
 - 6 pad layout relative to the other pad layout.
2. An assembly in accordance with claim 1, wherein the pad layout of
 - 2 the printed circuit assembly is offset relative to the pad layout of the area
 - array package pad layout.
3. An assembly in accordance with claim 2, wherein said pad layout
 - 2 of the area array package is in a regular grid pattern.
4. An assembly in accordance with claim 3, wherein said pad layout
 - 2 of the printed circuit assembly is offset with regularly spaced small groupings
 - of pads corresponding to the pads to be bonded on the area array package.
5. An assembly in accordance with claim 4, wherein the regularly
 - 2 spaced small groupings of pads on the printed circuit assembly comprise
 - four pads offset toward each other dispersed on the printed circuit assembly
 - 4 to correspond with the pads to be bonded on the area array package.

6. A method for manufacturing an assembly comprising:

2 obtaining an area array package having a pad layout pattern;
 obtaining a printed circuit assembly having a pad layout pattern
4 corresponding to the pad layout pattern of the area array package;
 and
6 attaching the area array package pad layout pattern to the printed
 circuit assembly pad layout pattern, wherein at least one pad layout
8 pattern is a regular grid pattern and the other pad layout pattern is offset
 relative to the regular grid pattern.

7. A method for detecting offset solder joint defects between solder
pads on an area array package attached to offset solder pads on a printed
4 circuit assembly, comprising the steps of:
 measuring a characteristic of an offset solder joint;
6 determining a value for an acceptable offset solder joint; and
 comparing the measured offset solder joint characteristic value with
8 the acceptable offset solder joint characteristic value.

8. A method in accordance with claim 7, further comprising the step
2 of:
 generating an error value for the solder joint.

9. A method in accordance with claim 8, further comprising the step
2 of:
 determining if the solder joint is defective.